**Lesson Plan**

**Name of faculty :** Ravinder Kumar Mehra

**Discipline :** Computer Engineering

**Semester :** 4th

**Subject :** Computer Organization & Architecture

**Lesson Plan Duration :** 16 Weeks (20 Jan to 15 May)

**Work Load (Lecture/ Practical) per week (in hours):** Lectures-04,

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| **Week** | **Theory** | |
| **Lecture day** | **Topic**  **(including assignment /**  **test)** |
| 1st | 1st | Hardware organisation of computer system  CPU organisation : general register organisation |
| 2nd | Stack organisation |
| 3rd | Instruction formats(three address, two address, one address |
| 4th | Zero address and RISC instruction) |
| 2nd | 5th | Addressing modes: Immediate, register, direct, in direct, relative, indexed |
| 6th | CPU Design : Microprogrammed vs hard wired control |
| 7th | Reduced instruction set computers:, |
| 8th | RISC characteristics, |
| 3rd | 9th | CISC characteristics and their comparison with RISC |
| 10th | 2. Memory organisation Memory Hierarchy |
| 11th | RAM Chips |
| 12th | ROM chips |
| 4th | 13th | Memory address map |
| 14th | Memory connections to CPU |
| 15th | Auxillary memory : Magnetic disks |
| 16th | magnetic tapes. |
| 5th | 17th | Associative memory |
| 18th | Cache memory, Virtual memory |
| 19th | Memory management hardware , |
| 20th | Read and Write operation |
| 6th | 21st | Sessional test-I |
| 22nd | 3. I/O organisation |
| 23rd | a. Basis Input output system(BIOS) |
| 24th | Function of BIOS o Testing |
| 7th | 25th | Function of BIOS o Testing and initialization |
| 26th | Configuring the system |
| 27th | b. Modes of Data Transfer o |
|  | 28th | Programmed I/O |
| 8th | 29th | Synchronous, asynchronous and interrupt initiated. |
| 30th | DMA data transfer |
| 31st | 4. Architecture of multi processor systems |
| 32nd | Forms of parallel processing |
| 9th | 33rd | Parallel processing |
| 34th | and pipelines |
| 35th | basic characteristics of multiprocessor |
| 36th | multiprocessors |
| 10th | 37th | General purpose multiprocessors’ |
| 38th | Interconnection networks |
| 39th | time shared common bus |
| 40th | time shared common bus |
| 11th | 41st | Sessional test-II |
| 42nd | multi port memory |
| 43rd | cross bar switch |
| 44th | Switch in memory |
| 12th | 45th | multi stage switching networks |
| 46 | hyper cube structures |
| 47 | hyper cube structures |
| 48 | switching networks revise |
| 13th | 49 | Introduction to I/O interface |
| 50 | Types of I/O Interface |
| 51 | Asynchronous Data Transfer |
| 52 | Revise |
| 14th | 53 | Synchronous Data Transfer |
| 54 | Strobe Control |
| 55 | Difference between Asynchronous & Synchronous |
| 56 | Serial Transfer |
| 15th | 57 | Handshaking Mechanism in DT |
| 58 | Describe Asynchronous Serial Transfer |
| 59 | Revise |
| 60 | Sessional Test-III |

RECOMMENDED BOOKS

1. Computer Architecture and Organisation by Moris Mano.

2. Computer Architecture by J. P. Hayes.

3. Structured Computer Organisation By Tanenbaum Andrew S, PHI. SUGGESTED

WEBSITES

1. http://swayam.gov.in

2. https://ekumbh.aicte-india.org